

FIG. 1 is a perspective view of a semiconductor device 100. The device includes a substrate 110 with a central chip 120. A first pad 130 is on the left, and a second pad 140 is on the right. A first wire bond 200 connects the first pad to the chip, and a second wire bond 300 connects the second pad to the chip. The chip has a central region 400 and peripheral regions 410, 420, 430, and 440. A cross-section line A-A is indicated.

FIG. 2

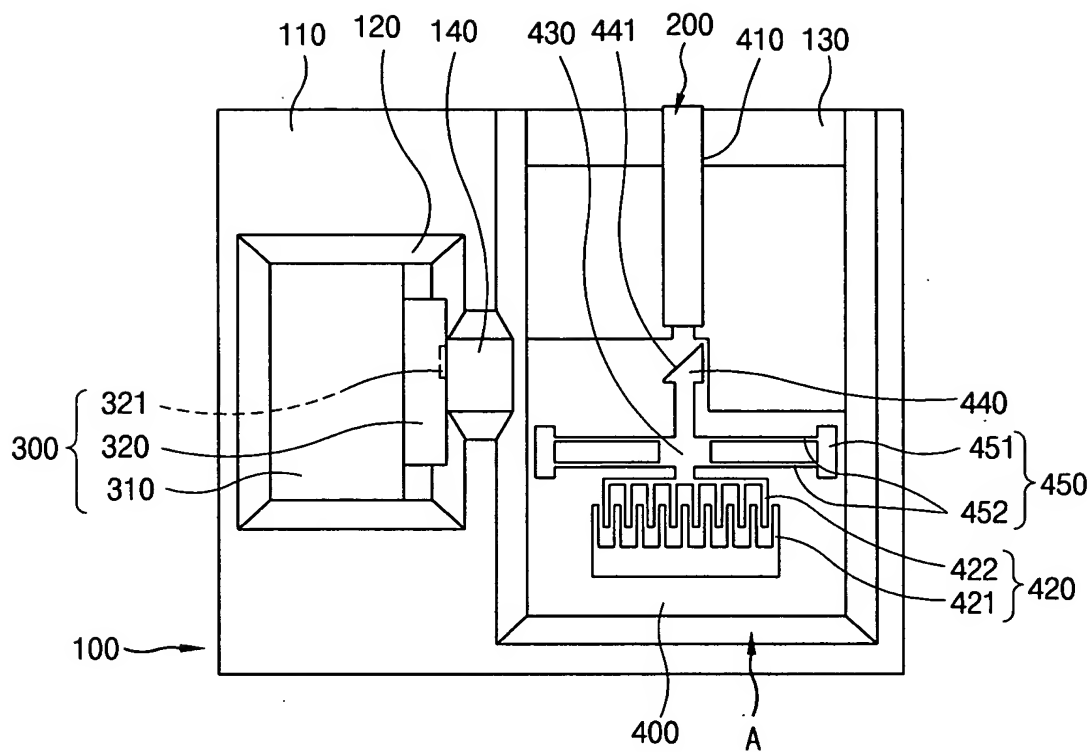


FIG. 3

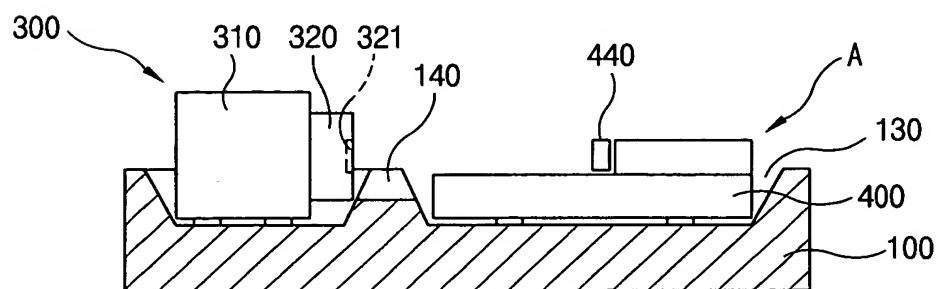


FIG. 4

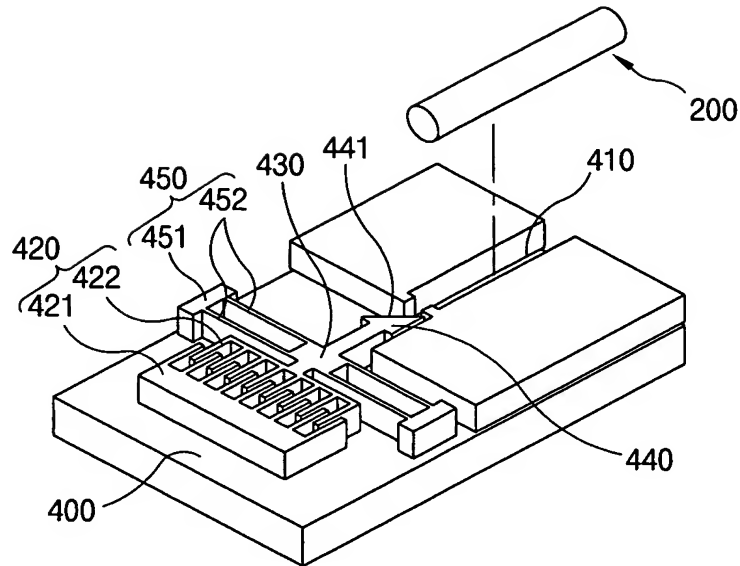


FIG. 5

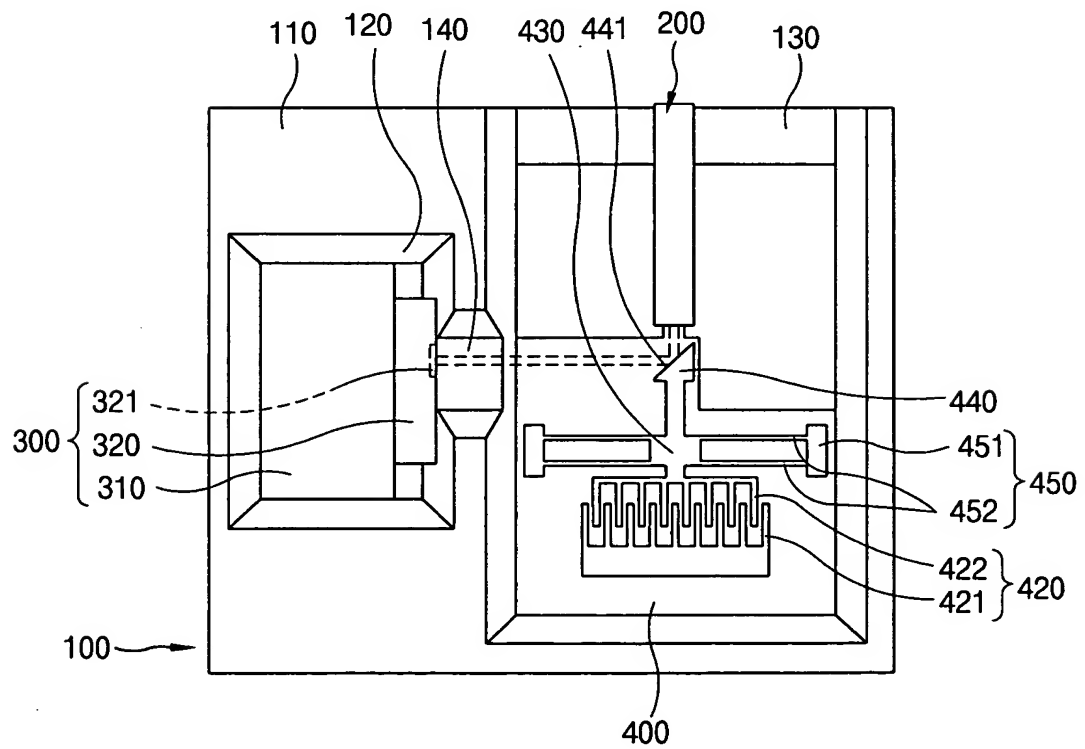


FIG. 6

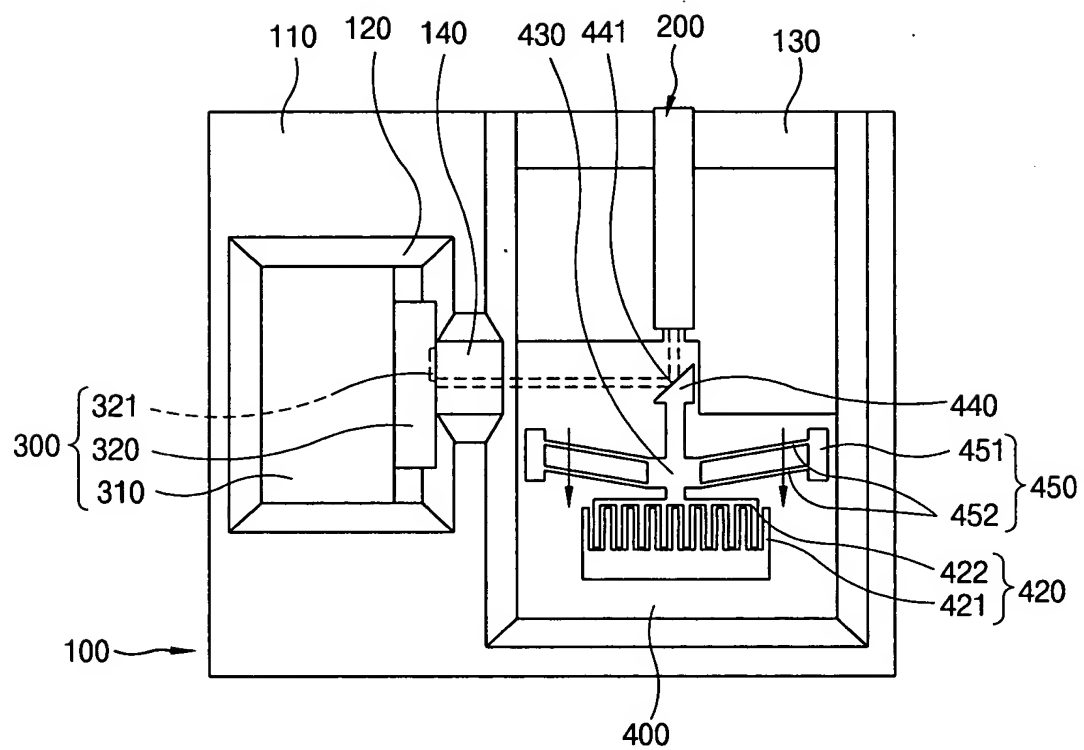


FIG. 7

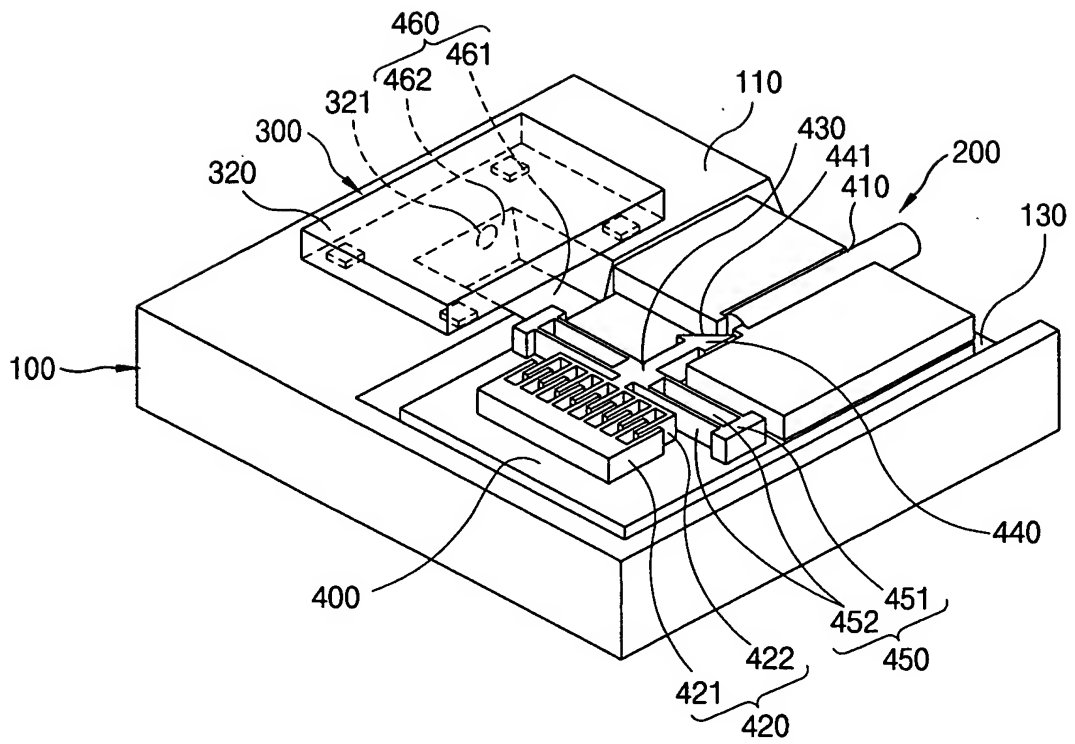


FIG. 8

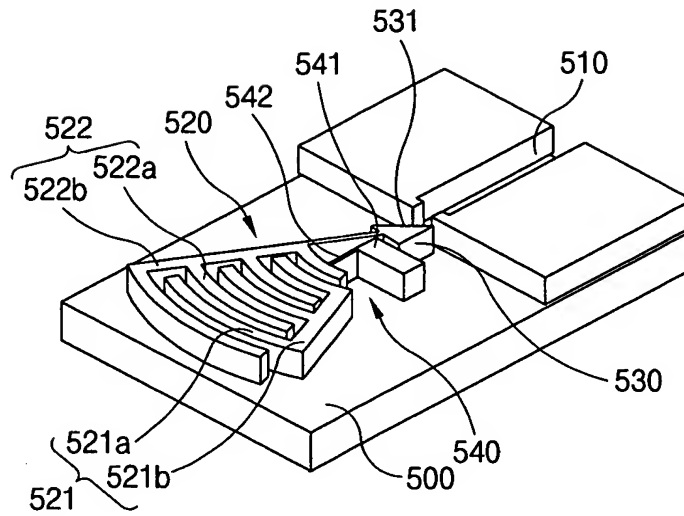


FIG. 9

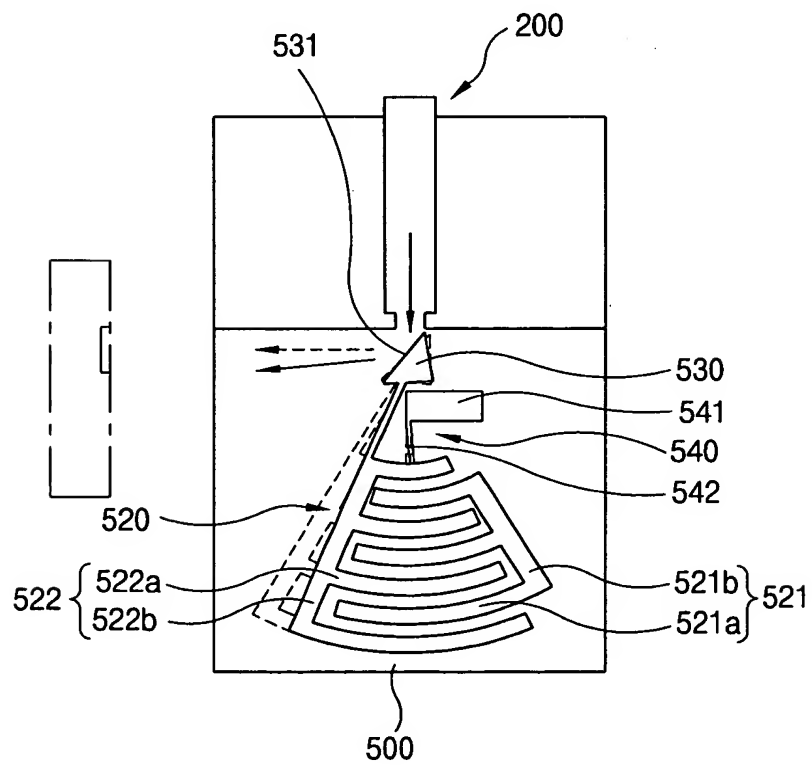


FIG. 10

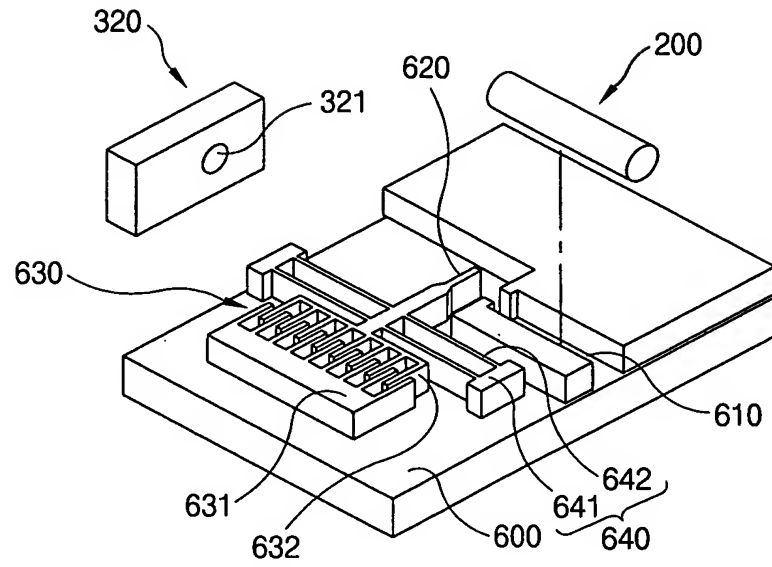


FIG. 11

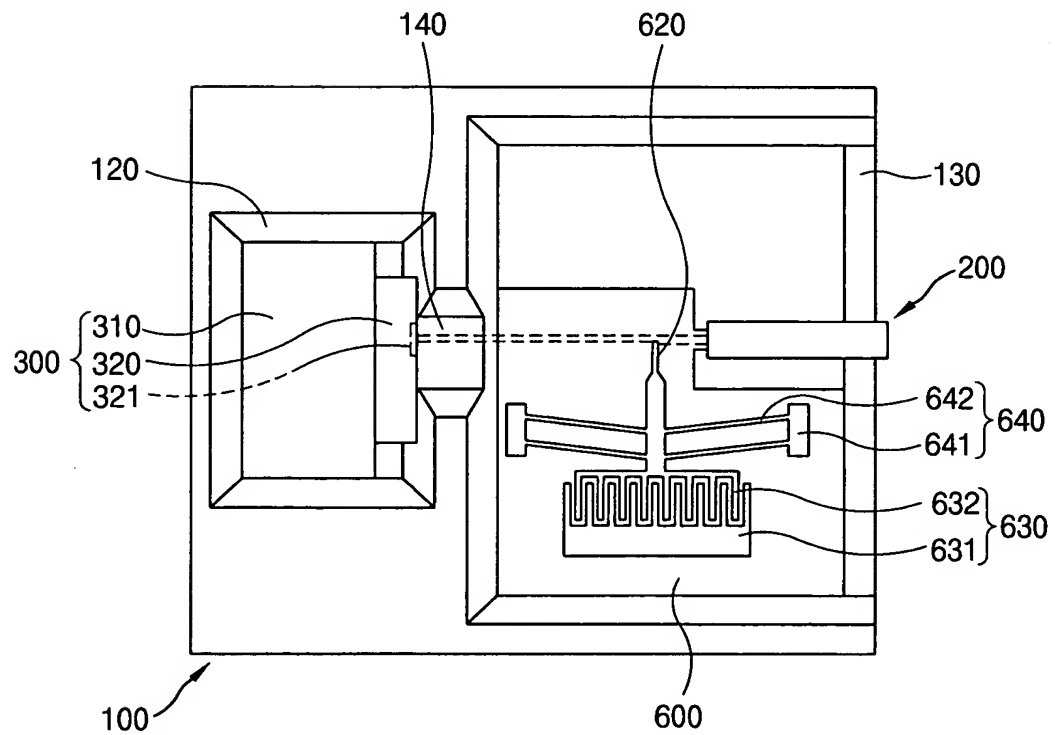


FIG. 12

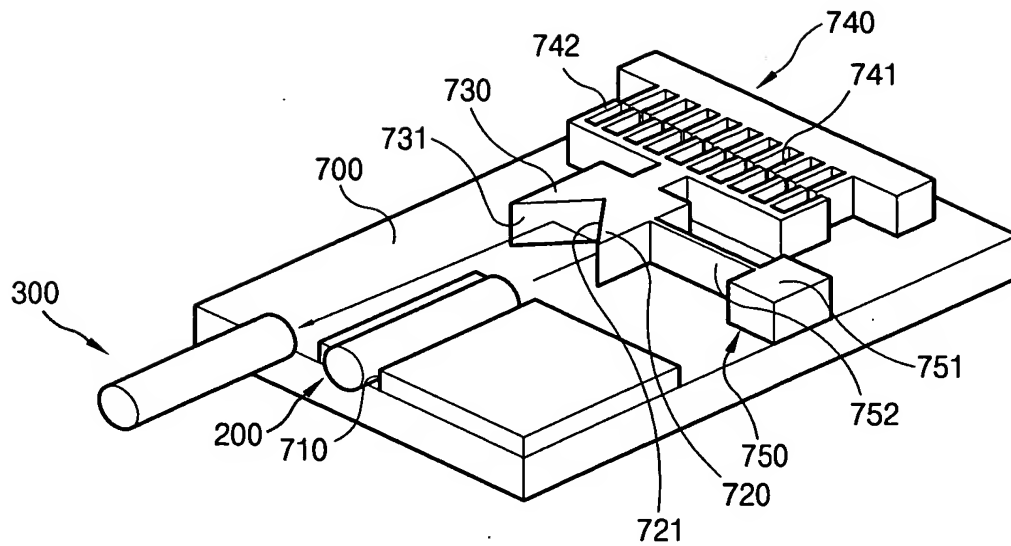


FIG. 13

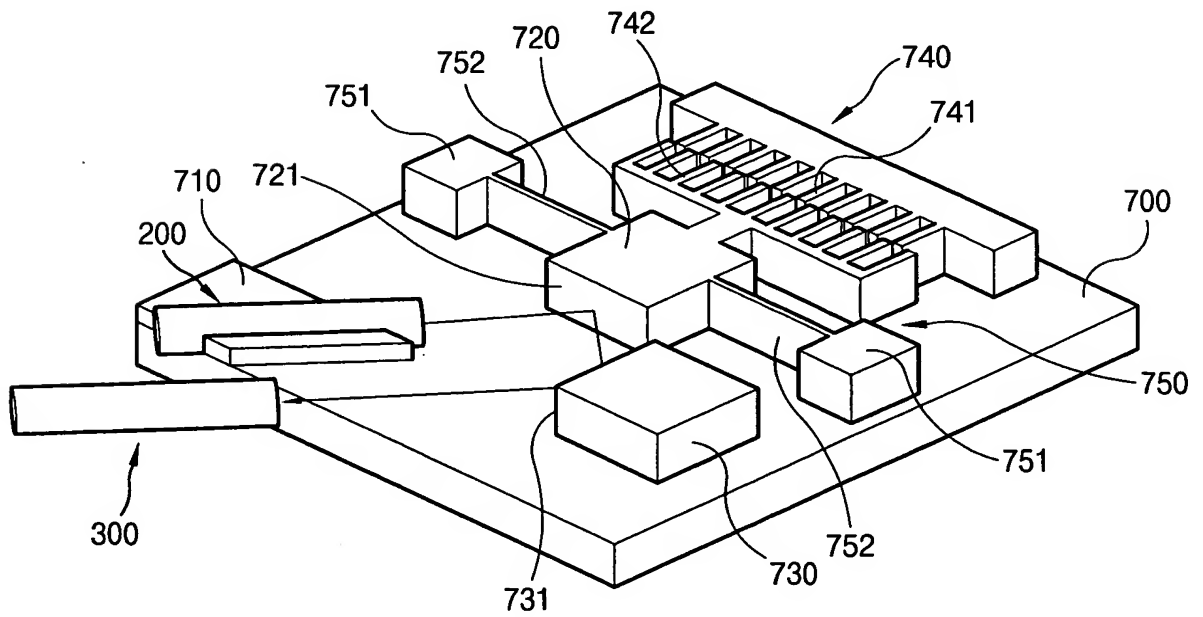




FIG. 14

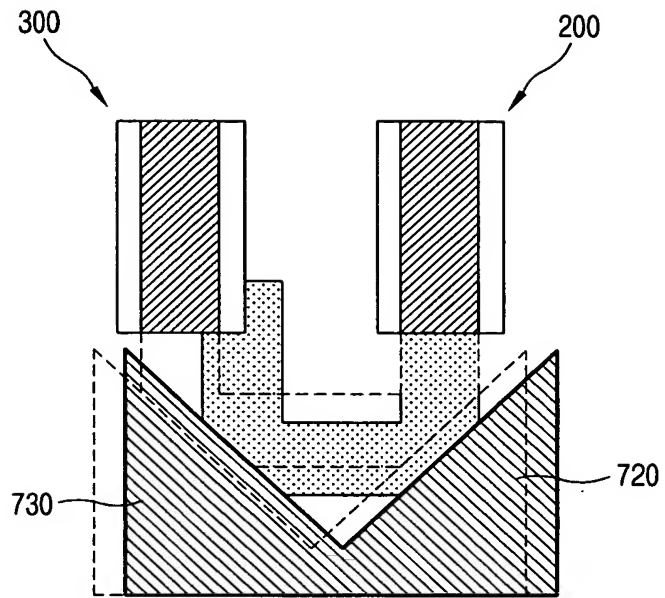


FIG. 15

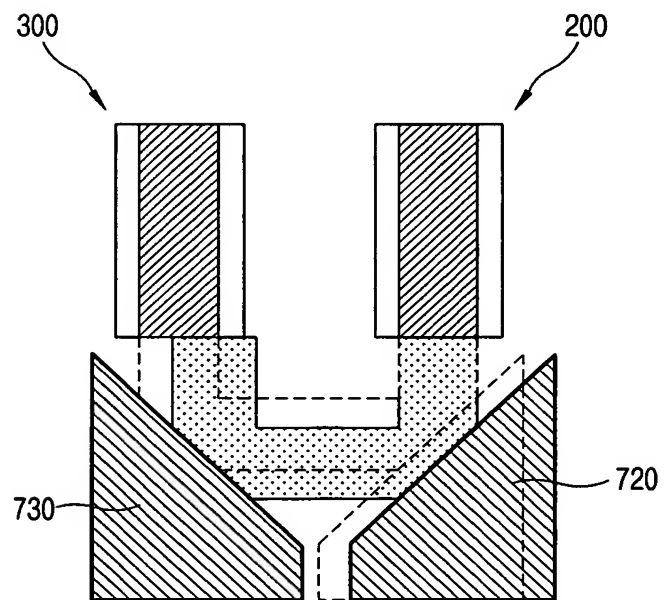


FIG. 16

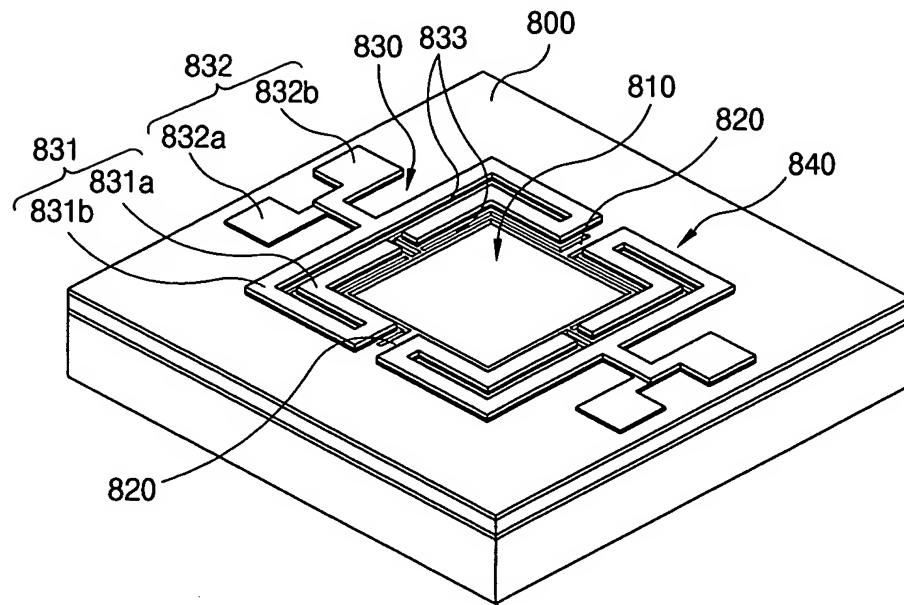


FIG. 17

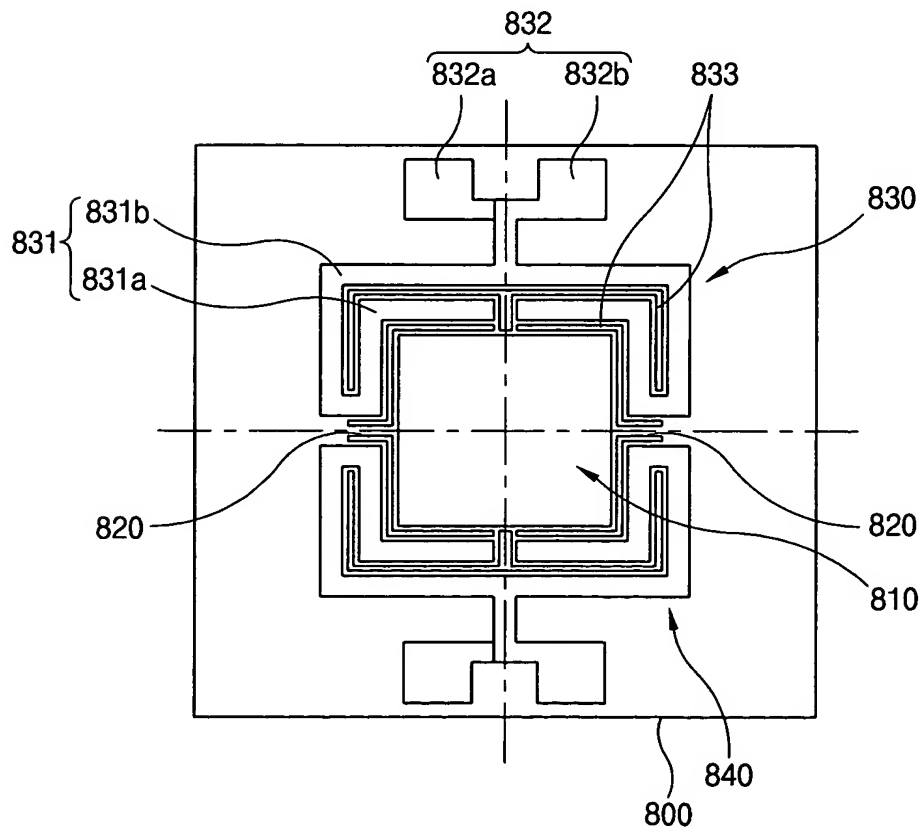


FIG. 18

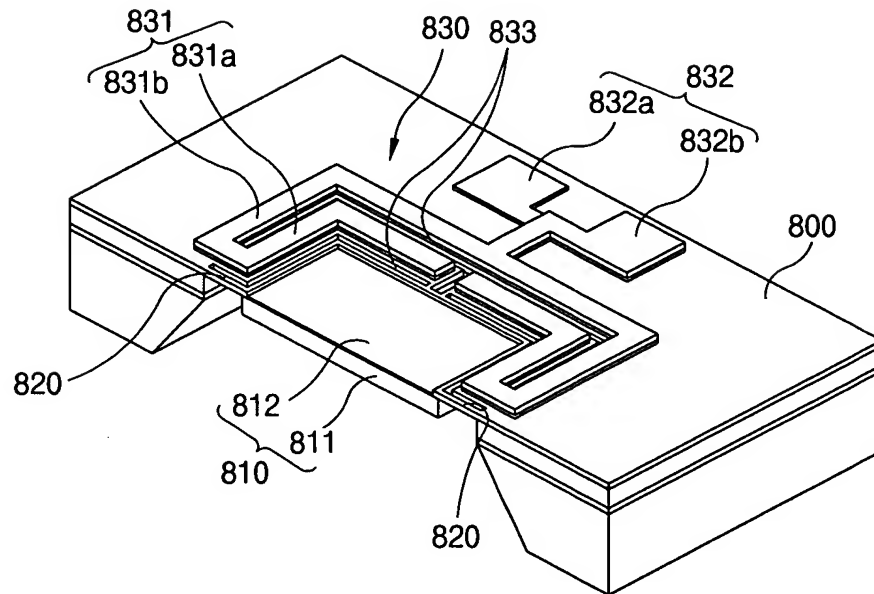


FIG. 19

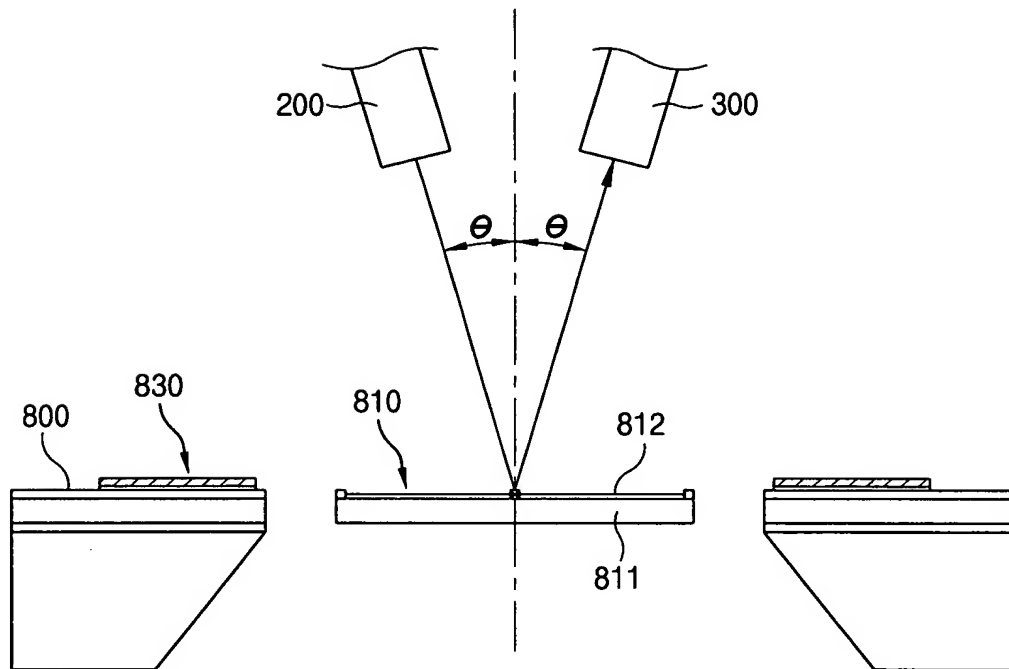


FIG. 20

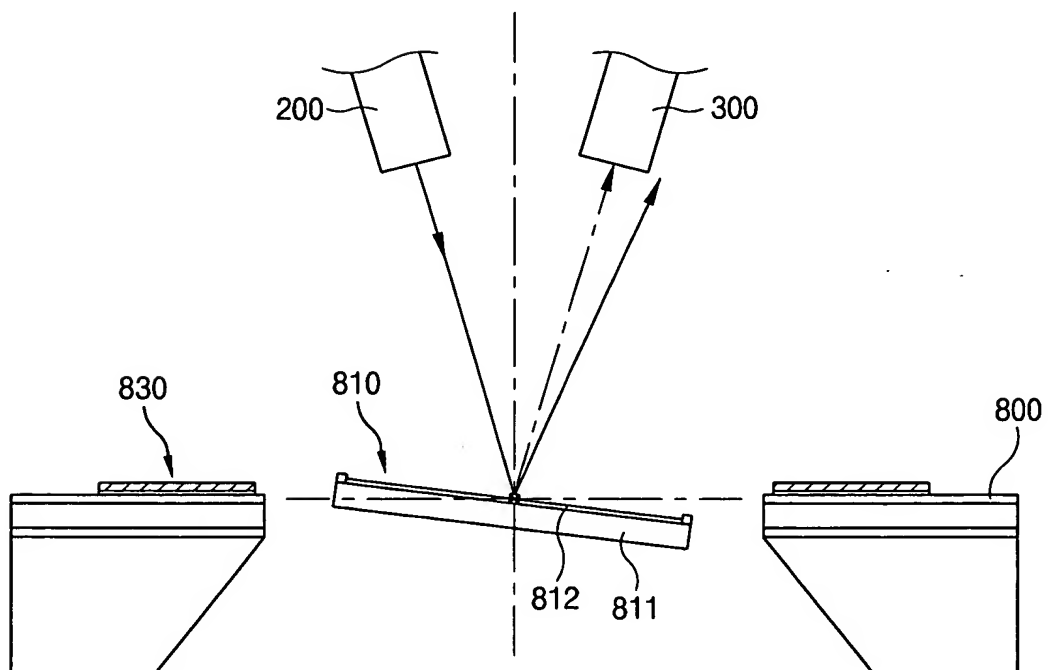


FIG. 21A

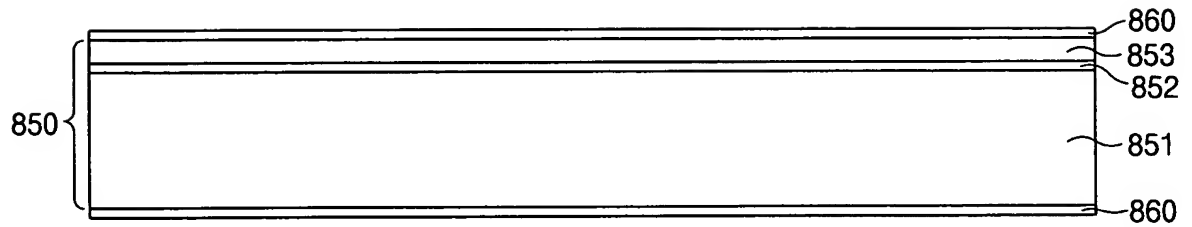


FIG. 21B

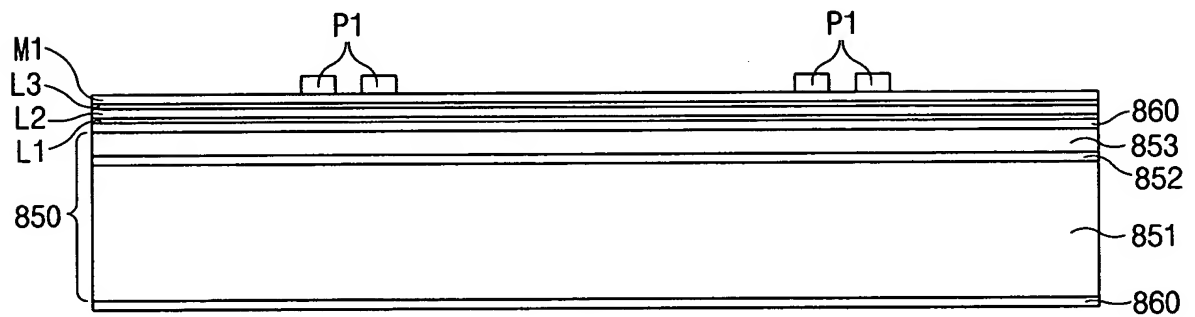


FIG. 21C

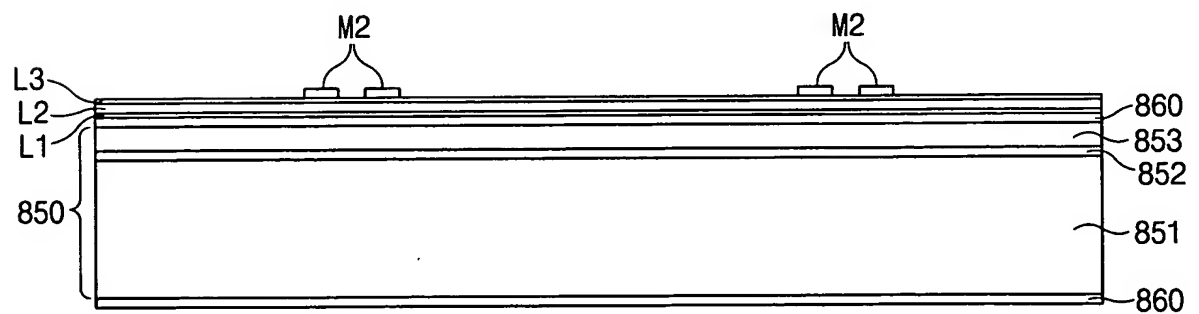


FIG. 21D

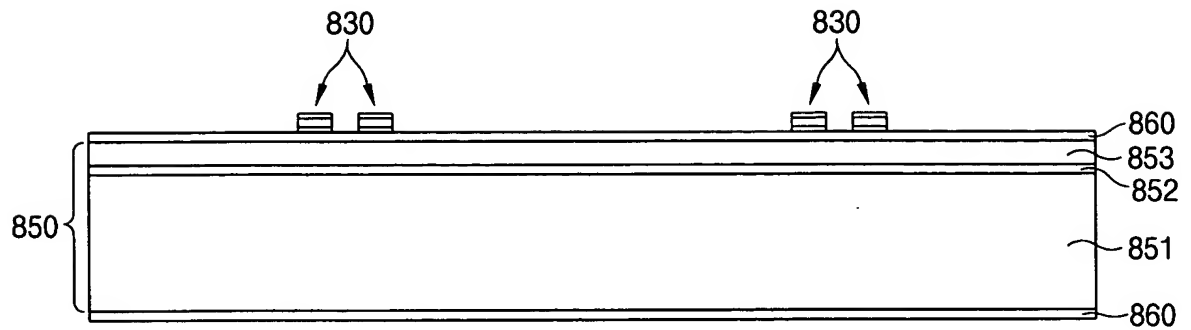


FIG. 21E

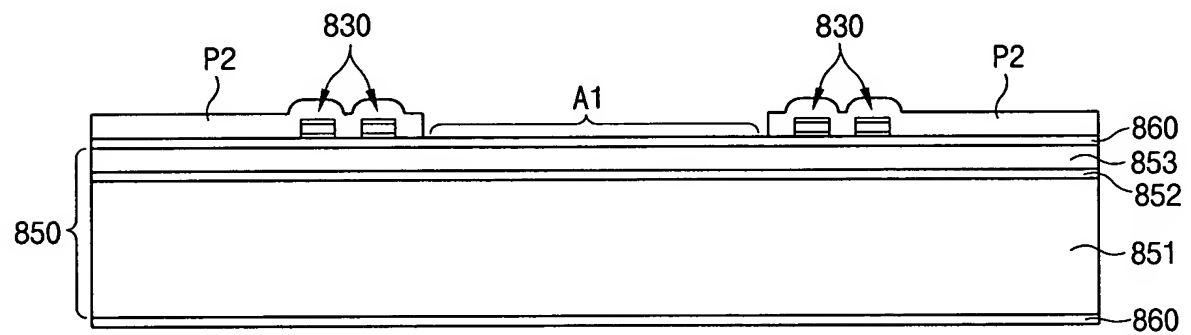


FIG. 21F

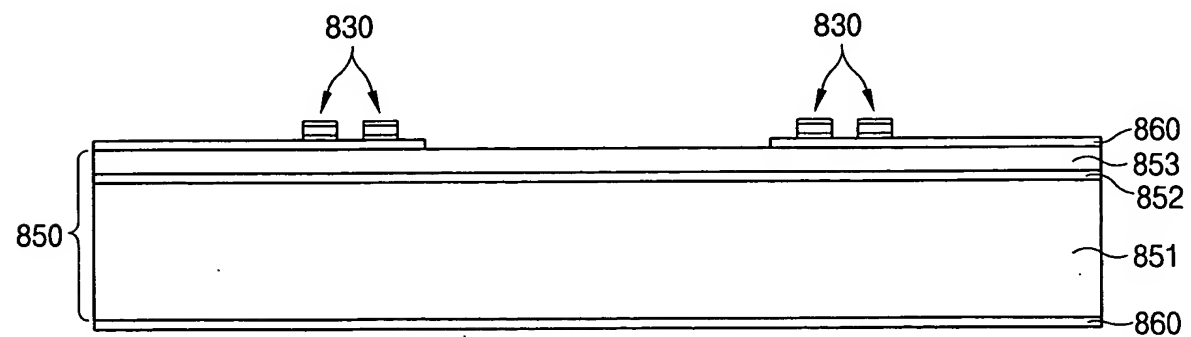


FIG. 21G

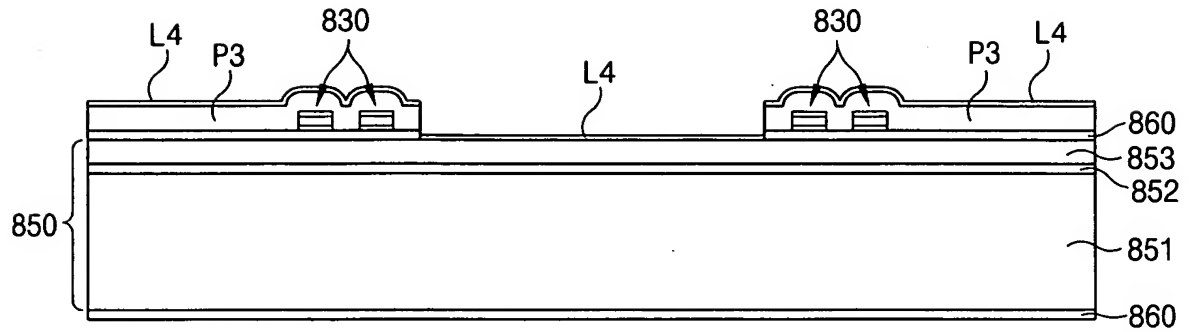


FIG. 21H

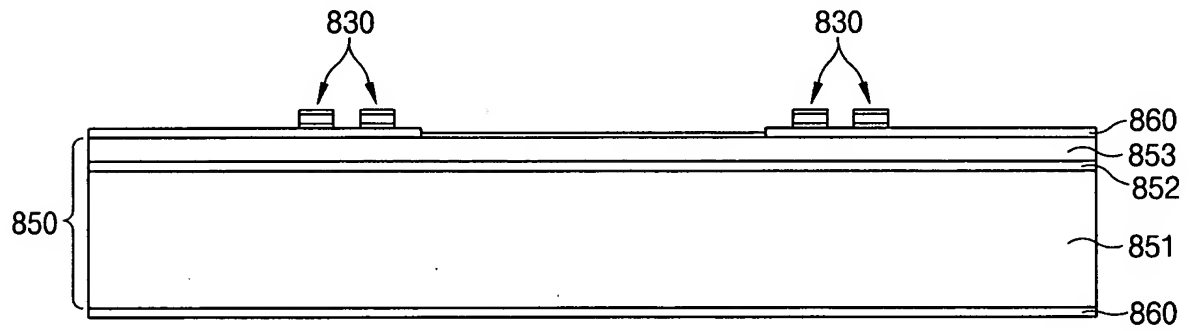


FIG. 21I

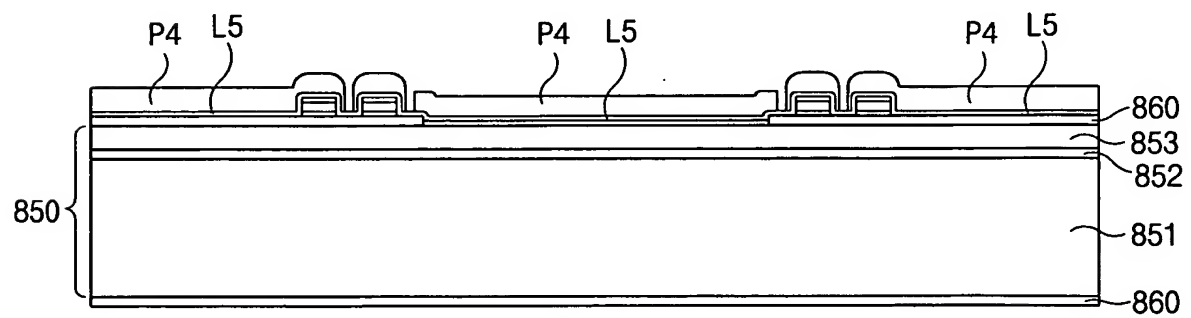


FIG. 21J

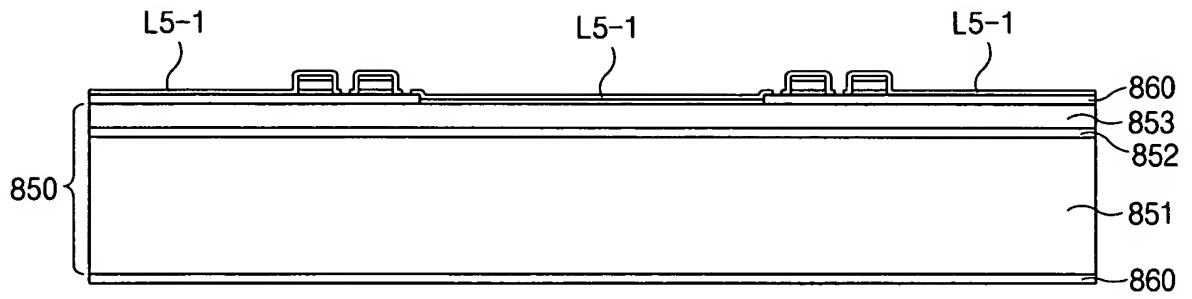


FIG. 21K

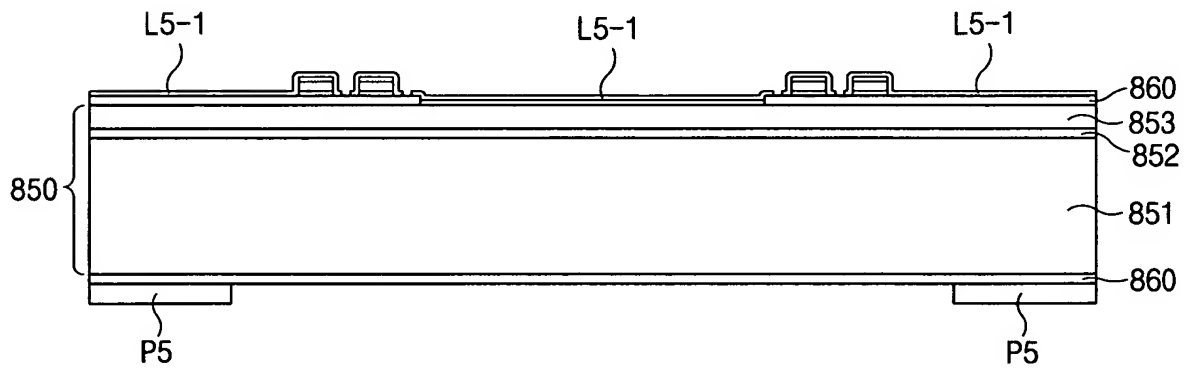


FIG. 21L

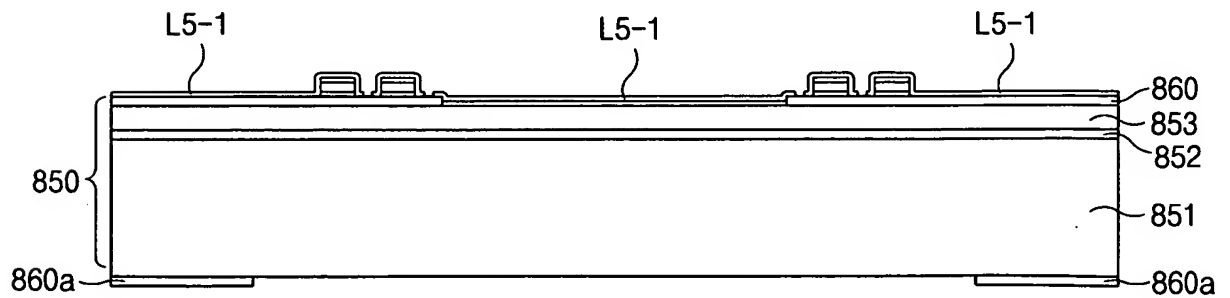




FIG. 21M

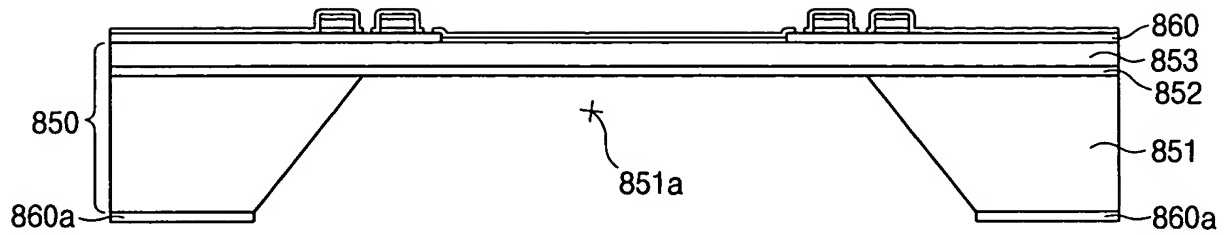


FIG. 21N

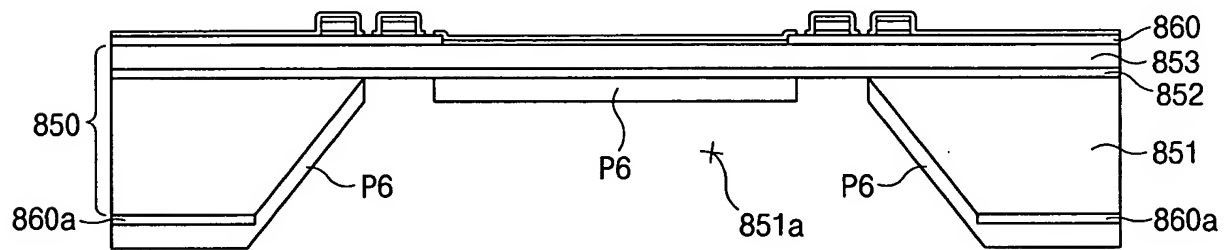


FIG. 21O

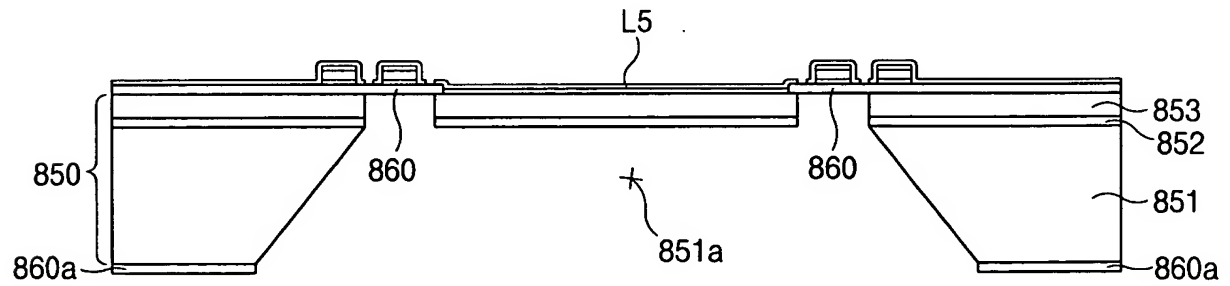


FIG. 21P

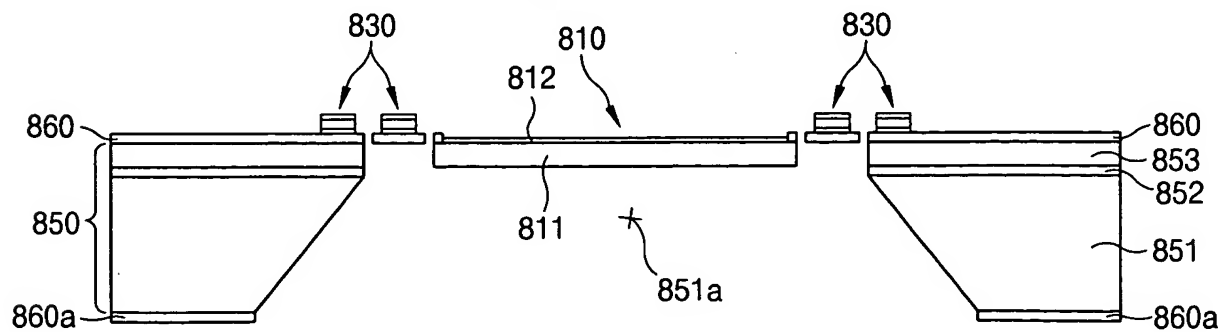


FIG. 22

